# Self-Assembling Silicon Nanowires for Device Applications Using the Nanochannel-Guided "Grow-in-Place" Approach

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**ABSTRACT** Silicon nanowires (SiNWs) have been grown with our nanochannel-template-guided "grow-in-place" approach and used in-place for resistor and transistor fabrication. In this methodology, empty nanochannels of a permanent template literally guide the vapor–liquid–solid (VLS) mechanism of SiNW growth and give control of the self-assembling nanowires' size, number, position, and orientation. The approach is demonstrated to give self-positioned/self-assembled SiNWs which are then used for device fabrication without any intervening SiNW collection, positioning, and assembling steps. These SiNWs may be grown so that they are extruded from, or confined within, the permanent nanochannel-template, as desired. The nanowire grow-in-place fabrication approach offers the potential for mass and environmentally benign manufacturing. The latter potential arises since only the exact number of nanowires needed is fabricated and these nanowires are always fixed at the position of use by the guiding nanochannels.

**KEYWORDS:** silicon nanowire · transistor · grow-in-place · self-assembling · guiding-nanochannel template · vapor–liquid–solid

One dimensional (1-D) nanoscale materials, such as nanowires and nanotubes, are emerging as interesting building blocks[1] for nanodevices in fields ranging from nanoelectronics to biosensors.[2] Among the promising nanoscale materials, silicon nanowires (SiNWs) appear particularly important because of their potential applications[3,4] in Si-based microelectronics and macroelectronics. To-date the overwhelmingly popular approach to producing these SiNWs has been some version of a "grow-and-place" fabrication methodology. These all use a growth step (the most popular being the vapor–liquid–solid (VLS) nanowire growth mechanism[5]), a collection (harvesting) step, and then a positioning and orienting step[6] on the final substrate in preparation for device fabrication. While grow-and-place approaches offer SiNWs with good size control,[7] the positioning and orienting steps of the SiNWs can present significant challenges. The most common approaches to these last steps have been "surface-patterning fluidic alignment"[8] and "electric-field assembly"[9] methods. In these techniques, the SiNWs are formed on a growth substrate, harvested, sorted for size and length, and then positioned and aligned using some combination of fluids and electric fields and subsequently fabricated into nanowire devices, such as transistors. Besides the multiplicity of cumbersome handling steps, the difficulty of obtaining acceptable interdevice packing for practical applications is another disadvantage of grow-and-place approaches. Two previous attempts to circumvent all these grow-and-place steps are found in the "patterned growth"[10] and "growth-in-trenches"[11] methods. The "patterned growth" was first proposed as a carbon nanotube growth-positioning approach.[10,12] It has been used also for Ge nanowires.[13] However, the patterned growth method does not give control over the number, direction, or interwire spacing of the nanowires produced. The "growth-in-trenches" approach offers a novel way to grow silicon nanowires (nanobridges) between two vertical silicon surfaces. In principle, the resulting nanowires can be used in place. However, the process can not control the number nor spacing of the SiNWs produced. In addition, the technique requires Si wafer substrates for creating the initiating, vertical Si growth surfaces.

In this report, we demonstrate that the various problems of the grow-and-place, patterned growth, and growth-in-trenches approaches can be avoided by using our nanochannel-template-guided "grow-in-place" methodology. We discuss the grow-in-place approach in detail and show that it offers a simpler and controlled, potentially manufacturable technology for nanowire

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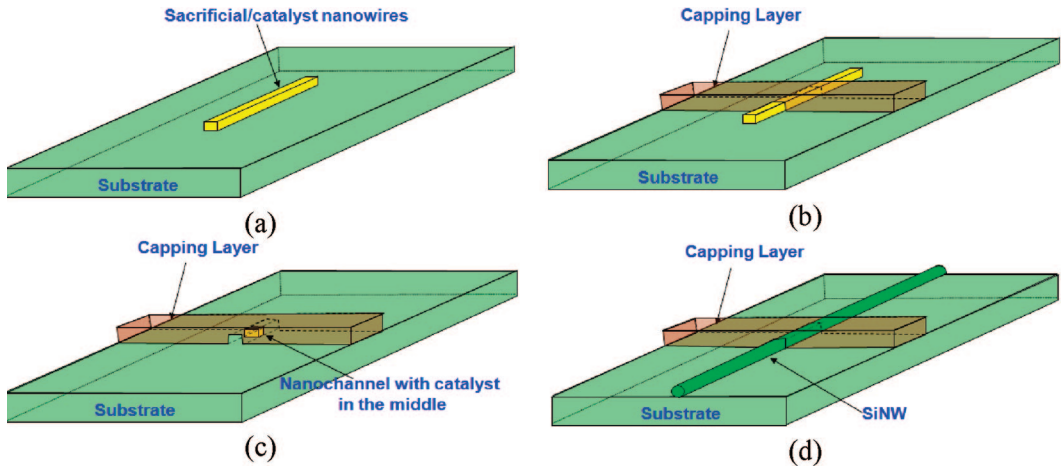


**Figure 1. Process flow for the fabrication of "grow-in-place" SiNWs using guiding nanochannel template: (a) sacrificial/catalyst metal (Au) line defined by e-beam lithography and lift-off; (b) patterning and deposition of the capping layer; (c) partial etching of the sacrificial metal to form empty nanochannels with catalyst in the middle; (d) Si nanowire growth and extrusion out of channel by the VLS mechanism.**

device fabrication. This presentation of SiNW growth and of subsequent device fabrication results is a further development and in depth discussion of our grow-in-place nanowire growth method introduced earlier.[14,15] The nanowire devices discussed are simple structures: single-wire four-point probe resistors and single-wire, top-gate SiNW unipolar accumulation metal oxide semiconductor field effect transistors (AMOSFETs).[15] In our grow-in-place approach the empty nanochannels present in a template "nurse" and guide the SiNW VLS growth, giving control of nanowire size, number, spacing, position and orientation. Depending on the details of the nanochannel length and the growth process, the resulting SiNWs can extrude form the template or be confined within the template, as required for the subsequent device fabrication sequence. With the grown SiNWs fixed by the nanochannels of the permanent template, nanowire devices, such as transistors, are then easily made from these well-controlled, positioned grow-in-place nanowires. We believe the grow-in-place fabrication approach is mass-manufacturable and environmentally benign[16] since the fabricated nanowires are always fixed by the guiding channels and only the exact number of nanowires needed is fabricated. In this report, we used nominally undoped SiNWs, grown using gold as the VLS catalyst, for making the resistor and AMOSFET structures. However, the fabricating of more complex devices such as MOSFETs requiring the inclusion of steps such as varying precursor gas composition or ion implantation for doping is straightforward. Further, the application of our grow-in-place approach is not limited to SiNW devices. Other nanowire or nanotube devices of different materials can be fabricated with this methodology by using different precursor gas, catalysts, and growth conditions.

To direct and control SiNW production in the grow-in-place approach, the template with its guiding growth-nanochannels must first be fabricated on a permanent substrate. For this work, substrates of silicon or glass were used. The template can be made by techniques such as electron-beam lithography or nanoimprinting. Here we used electron-beam lithography following the procedure of our previous work.[14,15] The sacrificial material used in template nanochannel formation was gold allowing it to also serve as the catalyst for VLS SiNW growth. The overall process flow for creating the template with its guiding growth-nanochannel is summarized in Figure 1. First, open trench(es) of desired size, number, orientation, and location were patterned by electron-beam direct writing on a resist film on a silicon-oxide-coated silicon substrate or a Corning 1737 glass substrate. Second, titanium (1.5 nm) was e-gun evaporated as an adhesion layer, and then gold was thermally evaporated to a desired nanometer thickness thereby defining the height of the nanochannel(s). Subsequently, the resist film was lifted off to reveal the gold line(s) positioned and spaced, as desired, on the substrate (Figure 1a). Third, a capping layer (*e.g.*, silicon oxide) with the designed width (*e.g.*, 3 $\mu$m in the case shown) was patterned by photolithography, silicon oxide deposition and lift-off (Figure 1b). Finally, the gold line(s), including the region buried under capping layer, were controllably removed by wet etching to form the empty nanochannels, as depicted in Figure 1c. For this process, a diluted Au etchant (type TFA from Transene Company, Inc.) was employed at room temperature, and the etching was stopped by immersion in DI water. A relatively short (*e.g.*, sub 1 $\mu$m) length of Au (slug) was retained in the middle of the otherwise empty channels to serve as the VLS catalyst for the SiNW growth (Figure 1c).

In the next step, VLS growth was carried out in a low pressure chemical vapor deposition (LPCVD) reactor at 500 °C and 13 torr, using 5% $SiH_4$ diluted in $H_2$ with a total flow rate of 100 sccm.[14,17] The template

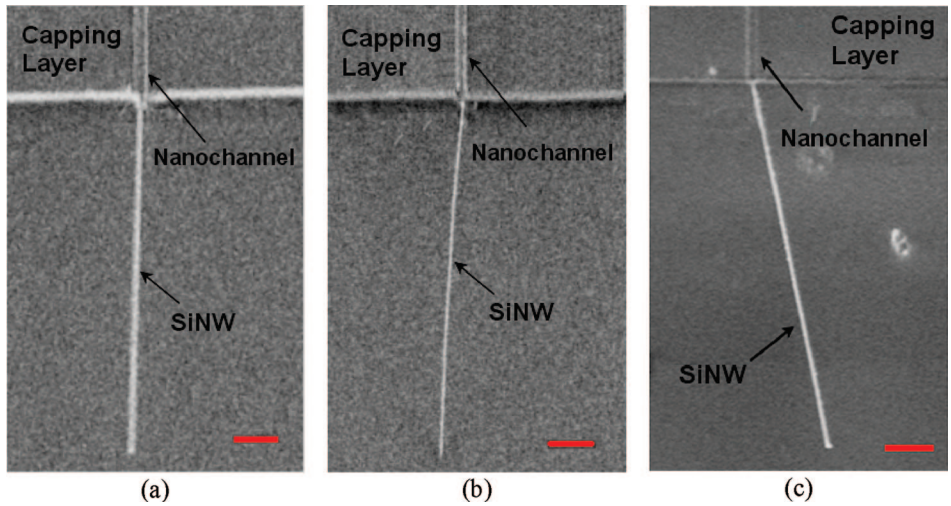


**Figure 2. FESEM images of SiNWs produced by the "grow-in-place" approach. Extrusion out of a guiding nanochannel is evident: (a) 150 nm width SiNW on glass substrate; (b) 80 nm width SiNW on glass substrate; and (c) 80 nm width SiNW on Si substrate.**

with its growth nanochannel guided the nanowire production by VLS as seen in Figure 1d resulting in unintentionally doped SiNWs. For the growth parameters and capping layer dimensions used, the SiNWs grew out of the guiding nanochannels (Figure 1d) at a growth rate of 1 $\mu$m/min (extrusion mode). Growth parameters and capping layer dimensions may be adjusted to confine SiNW growth to within the template, if so desired (confined mode). We allowed the nanowires to extrude in this report to a length of 15 $\mu$m to permit easy imaging and easy four contact, or gate and source/drain photolithographic definition, depending on whether four probe structures for resistivity-contact resistance studies or AMOSFETs were being fabricated.

Figure 2 shows field emission scanning electron microscope (FESEM) images of SiNWs which extruded from different cross-sectional sized nanochannels in this nanochannel-guided grow-in-place demonstration. Figure 2a shows SiNW of 150 nm in diameter, and Figure 2b shows SiNW of 80 nm in diameter, both grown on glass substrates. Figure 2c shows SiNW of 80 nm in diameter on silicon substrate coated with thermal grown silicon oxide. The FESEM images clearly show that SiNWs grew and extruded from the nanochannels. The prefabricated nanochannels defined the SiNW size, number, position, and growth orientation. After the nanowire growth, the residual gold on the nanowires was completely removed by rinsing the whole sample in gold etchant following by DI water cleaning. The SiNWs were then subjected to a modified standard cleaning.

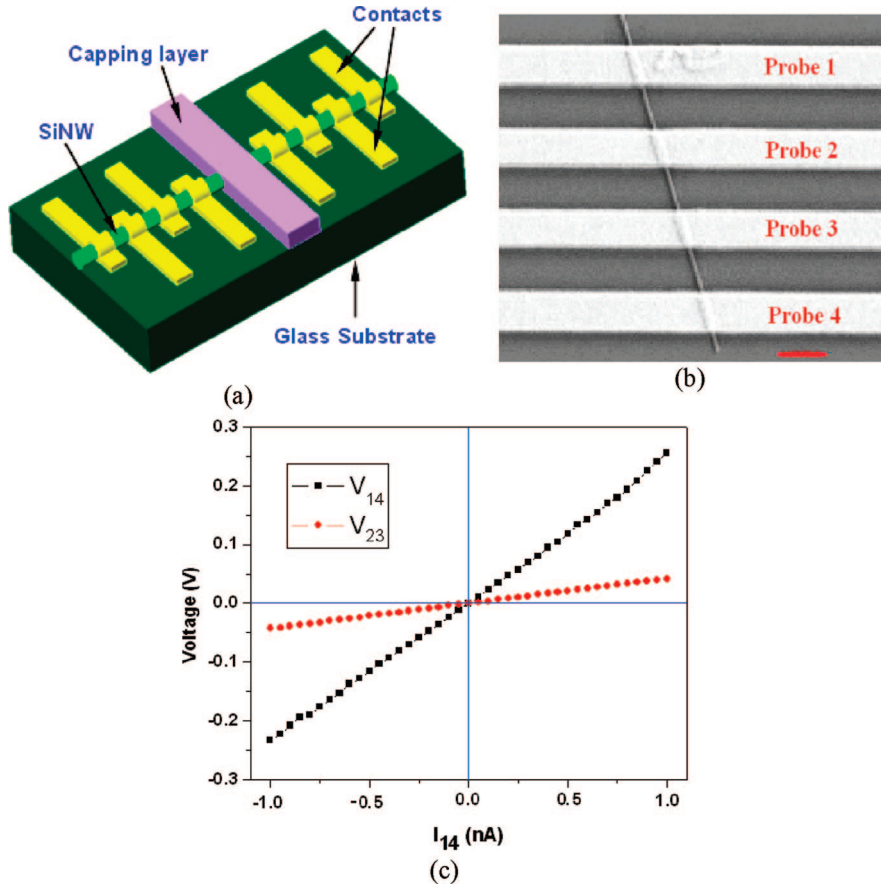


**Figure 3. Four-point probe measurement structure and diagram: (a) 3-D schematic of 4-point probe measurement structure; (b) FESEM picture of the structure. The SiNW diameter is 80 nm. The structure was defined by photolithography, with probe electrode width 1.5 um and spacing of 1.5 um. The electrode metal was Ti. The scale bar is 1 $\mu$m. (c) Four-point probe measurement diagram. The current $I_{14}$ was forced between probe 1 and probe 4 while the voltage drops $V_{14}$ and $V_{23}$ were measured.**

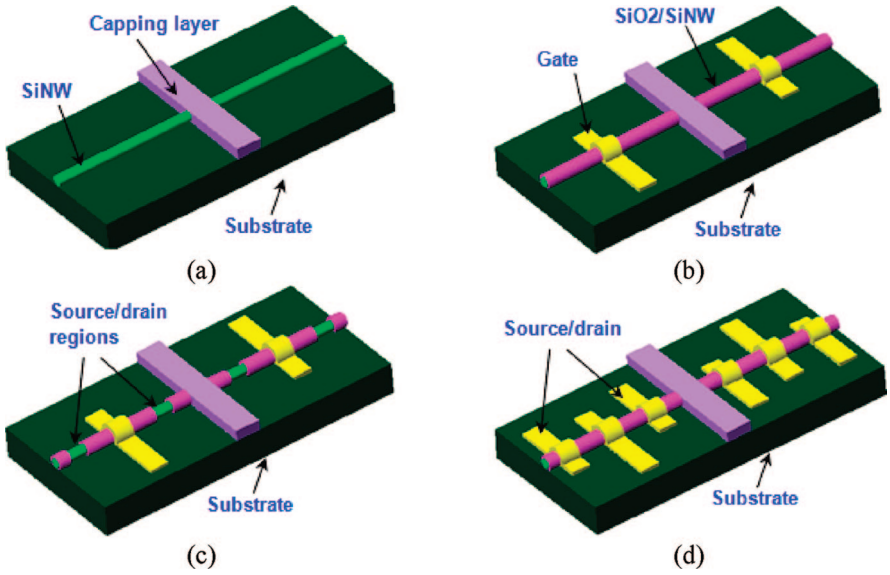


**Figure 4. Schematic representations of the top-gate core–shell SiNW transistor fabrication process. (a) SiNW after Au etching and cleaning, (b) SiNW oxidation and gate contact patterning, (c) Source/drain region patterning and oxide removal, (d) Source and drain contact deposition. In this depiction, two transistors are fabricated using an extruded nanowire.**

By using alignment markers and with the grown SiNW fixed and positioned by the nanochannel, a four-point probe resistor structure or FET can be easily fabricated from these well-controlled, self-positioned/self-assembled grow-in-place nanowires. For the devices discussed here, standard photolithography was utilized. E-beam or any other nanolithography could be used at this step but the principal point here is to discuss the grow-in-place methodology and the material it produces.

When making the four-point probe contact testing structure as shown in Figure 3a, photoresists LOR5A/SPR1805 were spun on, exposed, and developed. After removing the native oxide with an HF dip, the contacts (probes 1−4 of Figure 3a and 3b) were formed using a Ti (300 nm)/Au(40 nm) twin layer evaporated by e-gun depositions and defined by lift-off. A resulting four-point probe testing configuration is shown in a FESEM image (Figure 3b) for a SiNW diameter of 80 nm. In measuring the "bulk" resistivity of our grow-in-place SiNWs, we use probes 2 and 3 to yield the voltage drop $V_{23}$ while the current between probes 1 and 4 ($I_{14}$) was swept from −1.0 to +1.0 nA. The voltage drop $V_{14}$ between probe 1 and probe 4 was also simultaneously measured. The resulting current–voltage ($I-V$) plots in Figure 3c show that $V_{14}$ is somewhat more than 3 times $V_{23}$ indicating that the Ti/SiNW contacts do drop voltage for the 1 nA current range. However, these data show no Schottky barrier rectification[18–20] at our SiNW contacts. The $V_{23}$ *versus* $I_{14}$ plot (the red line in the Figure 3c) allows the "bulk" SiNW resistivity between probes 2 and 3 to be determined, independent of the contact voltage drop. The slope of this red plot gives the SiNW resistance $R_{s2-3}$ for the region between these probes as $R_{s2-3} = 4.26 \times 10^7$ ohms. From this value, the SiNW resistivity $\rho_s$ is calculated to be 14.3 ohm · cm (conductivity $\sigma_s = 0.07$ S/cm) using equation $R_{s2-3} = \rho_s L_{2-3}/\pi r_s^2$, where $L_{2-3} = 1.5$ $\mu$m is the spacing between the two middle contacts. This SiNW resistivity is close to that reported elsewhere for nominally undoped SiNWs produced using Au catalyzed VLS growth.[20] If we follow Maiolo *et al.* (ref [21]) and use bulk Si mobility values for SiNWs, the resulting carrier density is $9 \times 10^{14}$ cm$^{-3}$. As shown below with the transistor characterization, these carries are holes.

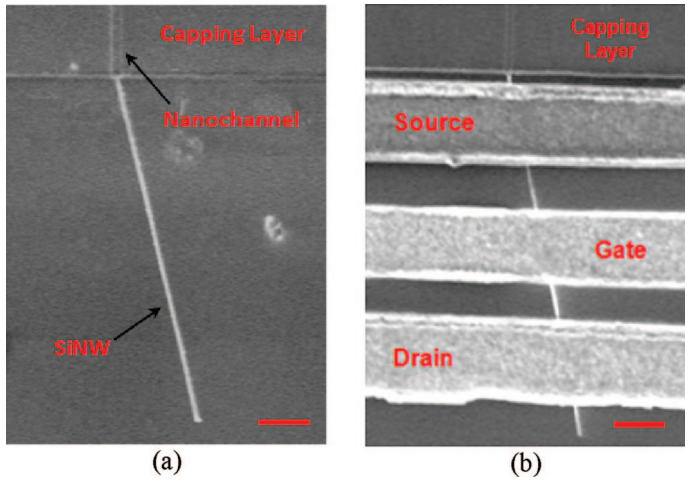


**Figure 5. SiNW AMOSFET transistor: (a) grow-in-place SiNW before transistor fabrication; (b) the corresponding SiNW transistor after gate and source/drain patterning.**

When FETs were made from the grow-in-place SiNWs, we chose to fabricate AMOSFET devices owing to their simplicity.[14] In fabricating these devices (Figure 4a), an encapsulating $SiO_2$ layer was first grown on the nanowires by dry thermal oxidation[22] at 700 °C for 4 h[22,23] using a 3 L/min $O_2$ flow rate. This oxidation resulted in a Si/$SiO_2$ core–shell structure[22–25] with ~10 nm thermal silicon oxide surrounding the SiNWs (Figure 4b). This thermal oxide becomes the FET gate dielectric and it also serves to passivate the SiNW surface and reduce SiNW surface-state density. Second, the gate electrodes of the SiNW FET structures were then fabricated on these core–shell SiNW/$SiO_2$ structures by spinning on the twin-layer photoresists (LOR5A/SPR3012) and opening up the gate region through photolithography. The gate contacts were formed as shown in Figure 4b by metals Ti (400 nm)/Au (50 nm) deposition and lift-off. Third, the source/drain contacts were then fabricated on these core–shell SiNW/$SiO_2$ struc-

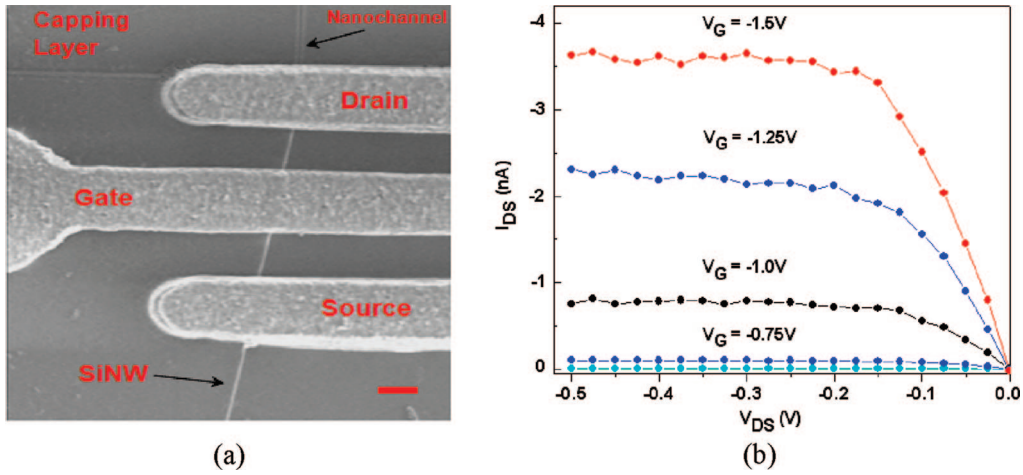


**Figure 6. A SiNW AMOSFET transistor and its output characteristics: (a) the testing structure and (b) the corresponding output characteristics, $I_{DS}$ *versus* $V_{DS}$ diagrams with $V_G$ from −1.5 to +0.5 V in 0.25 V steps from top to bottom.**

tures in a similar way, but with oxide removal. The twin-layer photoresists (LOR5A/SPR3012) were spun on and the source and drain regions were opened. The photoresist layer in this step served as a mask for etching the silicon oxide around the SiNW core as well as defining source/drain contacts. After the silicon oxide surrounding the SiNW core in the source/drain regions was etched (Figure 4c), the contact metals (400 nm Ti/50 nm Au) were deposited with the Ti contacting the SiNW, followed by lift-off (Figure 4d).

Figure 5a shows a FESEM image of our grow-in-place SiNW before AMOSFET transistor fabrication and Figure 5b shows the corresponding finished AMOSFET transistor structure. From FESEM micrographs, it can be concluded that the diameter of the oxidized SiNW is ~80 nm. It has been estimated by other investigators that the thickness of the oxide shell surrounding the SiNW for the oxidation parameters used is 10 nm. These results establish that the SiNW diameter is ~60 nm. TEM characterization of SiNW oxidation done by these other investigators has shown very good oxide/SiNW interface quality.[22]

The transistor performance characterization for AMOSFETs such as those seen in Figures 5b and 6a was carried out using an Agilent 4156 Precision Semiconductor Parameter Analyzer. Figure 6b shows the current ($I_D$) *versus* drain-source bias voltage ($V_{DS}$) (output characteristics) data for one single SiNW with source/drain electrodes and top gate electrode. The gate width for the device was 2 $\mu$m and the spacings between gate and source/drain electrodes were 2 $\mu$m. This nominally undoped SiNW AMOSFET data are shown at different values of the gate voltages ($V_G$). The $I_D$–$V_{DS}$ curves show that the drain current $I_D$ first increases in magnitude and then saturates with increasing negative drain voltage ($V_D$). The family of the $I_D$-$V_{DS}$ shows that the magnitude of $I_D$ increases with the negative increase of $V_G$ from 0.5 to −1.5 V. These data indicate that SiNW transistors produced by the processing described behave as p-type material, unipolar AMOSFETs.[14]

The corresponding semilog plot of log $|I_D|$ *versus* $V_G$ (transfer characteristics) with $V_D$ fixed at −0.1 V is shown in Figure 7 as the red curve (scale on the right ordinate). This figure also incorporates a linear plot (black curve) of $I_D$ *versus* $V_G$ (scale on the left ordinate). From the semilog (red) plot, the device is seen to have an on/off ratio of $10^6$ and a subthreshold slope ($S$) of 130 mV/dec. Although this latter value is approximately double the best value in single crystal silicon devices (70 mV per decade),[18] we believe this subthreshold slope is lower than the typical values reported for single, top-gate or bottom-gate silicon nanowire devices.[6,13,20] This $S$ value is also comparable to the best value (120 mV/dec) seen for vertical silicon nanowire array devices. In addition, this value is lower than the best values obtained for poly Si TFTs (200 mV per decade).[26]

The SiNW FET structure of Figure 6a has a threshold voltage of −0.6 V as seen in Figure 7 and requires a negative $V_G$ to turn on, showing that the channel is in

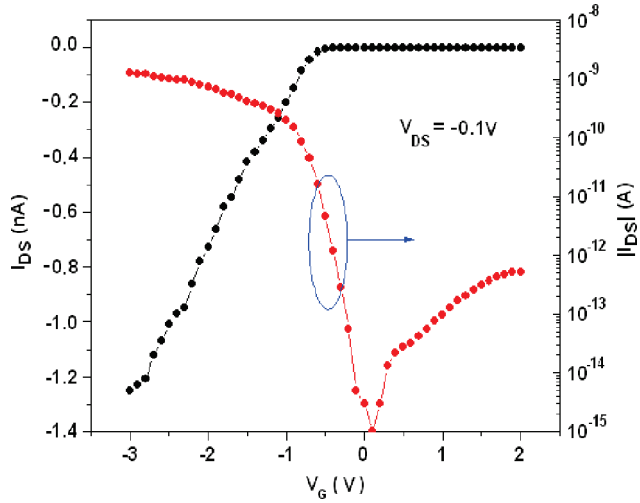


**Figure 7. SiNW AMOSFET transistor transfer characteristics of device shown in Figure 6a.**

the off-state with zero gate voltage. This indicates that the low work function metal Ti, used as the gate, possibly in conjunction with the usual fixed positive charges expected in a low temperature oxide,[18] must deplete the SiNW "bulk" holes beneath the gate. The picture that inadvertent doping during the VLS process has rendered the SiNW p-type, is consistent with our earlier contact studies[14,15] and other reported results.[27] The overall behavior means that the negative $V_G$ values in Figures 6b and 7 restore the "bulk" holes absent at $V_G = 0$ V and can also, with sufficient negative gate bias, induce a "surface" accumulation layer of holes under the gate.[14] As can be seen from a comparison of Figures 3c and 6b, for a given $V_{DS}$ value, sufficient negative gate voltage restores the SiNW current to the values it had before hole depletion. The AMOSFET device model is discussed in detail in ref 15.

In summary, we have discussed in detail our nanochannel-template-guided "grow-in-place" approach and have demonstrated it for extruded SiNWs. The grow-in-place method offers the ability to directly synthesize self-positioned/self-assembled SiNWs for device fabrication without any intervening silicon material formation, collection, positioning, and assembling steps. Taking four-point probe resistor and AMOSFET structures as examples, we made SiNW devices with no postsynthesis collection, nanowire alignment, and assembly steps and thereby avoided the difficulties present when making nanowire devices using grow-and-place methods. We believe our demonstration and discussion support the proposition that the grow-in-place methodology has significant potential as an environmentally benign, manufacturable approach.

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